Abstracts

Integrated inductors in the chip-to-board interconnect layer fabricated using solderless electroplating bonding

Yeun-Ho Joung, S. Nuttinck, Sang-Woong Yoon, M.G. Allen and J. Laskar. "Integrated inductors in the chip-to-board interconnect layer fabricated using solderless electroplating bonding." 2002 MTT-S International Microwave Symposium Digest 02.3 (2002 Vol. III [MWSYM]): 1409-1412 vol.3.

Integrated inductors are typically formed either on-chip or embedded in the chip package or board. In this work, we explore the possibility of forming inductors in the chip-to-board interconnect layer. The solderless technique of electroplating bonding is used to simultaneously form inductor structures as well as chip-to-board interconnect The use of the gap between the chip and substrate for inductors not only increases integration density, but also allows large magnetic cross-sectional areas to be achieved. To demonstrate the technology, 3- and 7-turn inductors 500 /spl mu/m in height were fabricated. These inductors showed inductance values of 3.45 nH and 10.5 nH, respectively. The measured Q-factors of the 3- and 7-turn inductors were 70 and 55 respectively, which agreed very well with modeling results.

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